CS303 – Logic & Digital System Design

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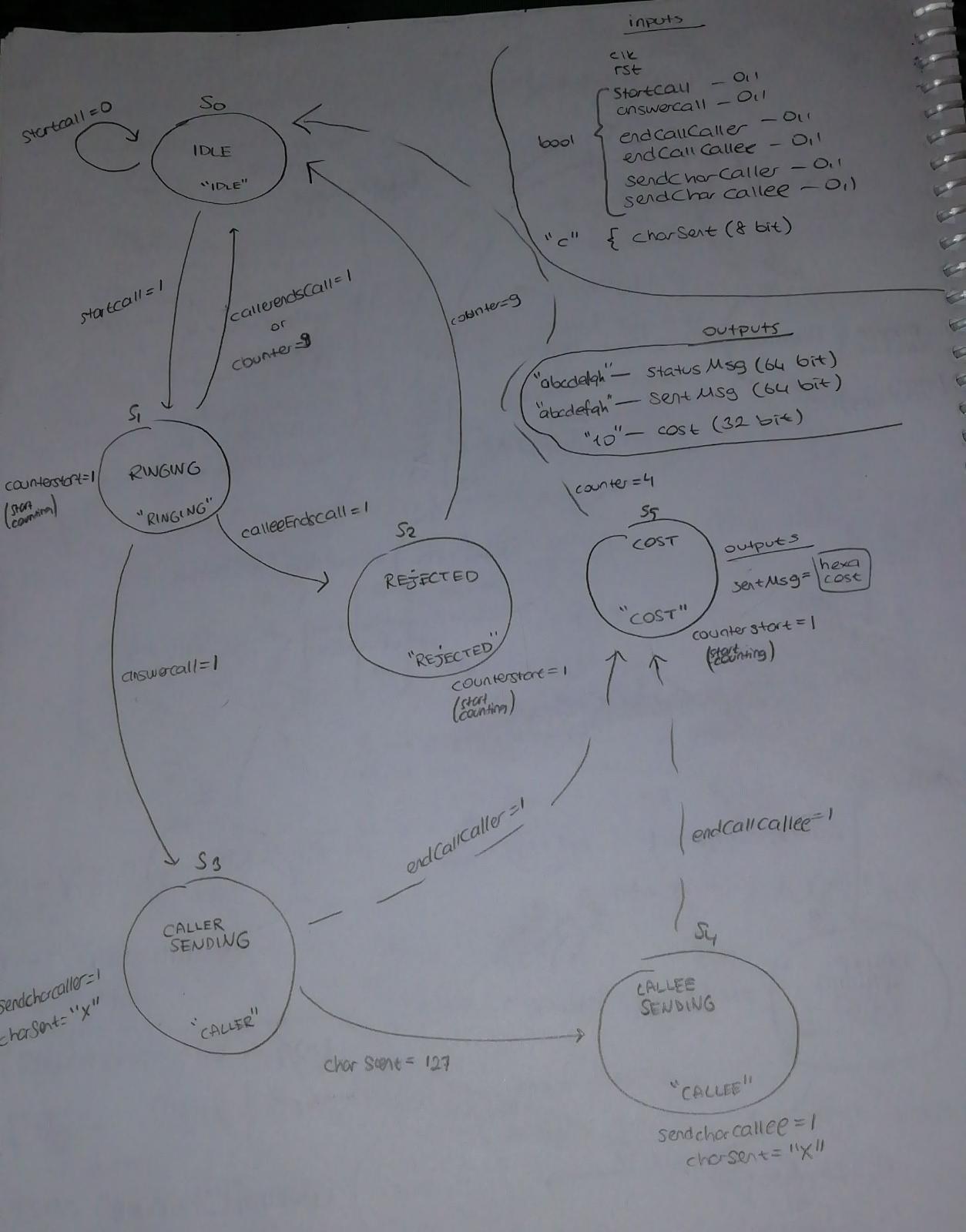
Student ID: 27017

**Overview**

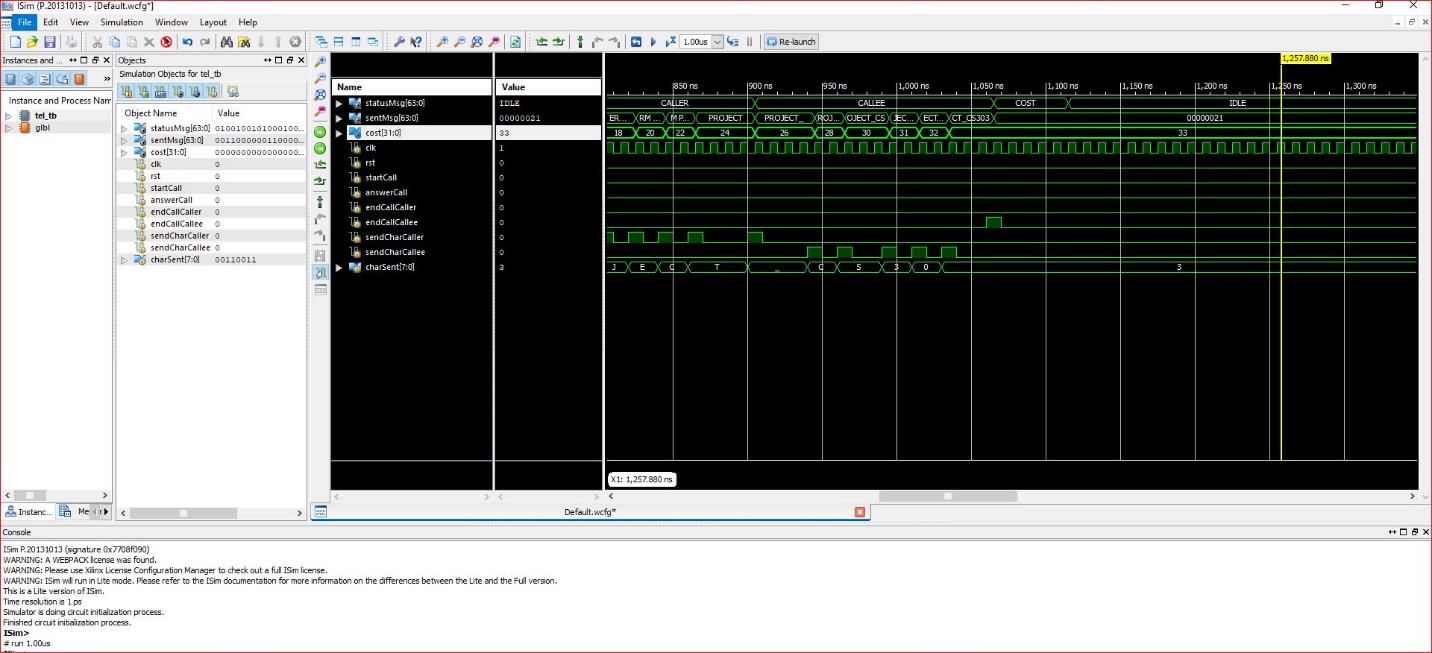
In this project, I’ve designed a sequential circuit for a simple two-sided telephone conversation and implemented it using Verilog HDL Basically, the caller will initiate a telephone conversation with the callee and the caller will send characters to the callee (and vice versa). My circuit also calculates the cost of the call and sends the cost value and the characters (sent from the caller to callee and vice versa) as outputs.

I have 6 states which are labeled as:

1. S0 = IDLE
2. S1 = RINGING
3. S2 = REJECTED
4. S3 = CALLER\_SEND
5. S4 = CALLE\_SEND
6. S5 = COST



P.s. : I have an extra output of “cost” which is with radix unsigned decimal that shows the real number of cost in decimals. (I wanted to check if it calculates correctly or not.)

**SIMULATION**

The given test case seems to be working fine.

**Synthesis results**

Number of 4-input LUT’s : 157

Timing Summary:

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Speed Grade: -4

Minimum period: 7.875ns (Maximum Frequency: 126.984MHz)

Minimum input arrival time before clock: 8.503ns

Maximum output required time after clock: 7.107ns

Maximum combinational path delay: No path found